Application No.: 10/035,186 Docket No.: 21806-00146-US

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-13 (Canceled).

14. (Currently Amended) A method for testing external C4 connections to ~~a~~ digital semiconductor devices at the wafer level, the method comprising:

providing an external electrical path via a thin film interposer probe between a selected subset of external C4 connections on the digital semiconductor devices; and

carrying out the testing by sending at least one signal through the external electrical path,

wherein the testing comprises at least one of a boundary scan and an input/output wrap test.

15. (Canceled).

16. (Original) The method according to Claim 14, further comprising:

pairing all adjacent input/output pairs.

17. (Withdrawn) The method according to Claim 14, wherein the test comprises a high frequency closed loop self test of drivers and receivers.

18. (Withdrawn) The method according to Claim 14, wherein the test comprises burn-in.

19. (Original) The method according to Claim 14, further comprising:

interfacing a driver from an input/output to a receiver of a corresponding paired input/output.

20. (Original) The method according to Claim 14, wherein providing the external electrical path comprises:

providing a thin film of electrically insulating material;

providing a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;

providing electrically conducting material arranged in the plurality of passages; and

providing electrical connections between the electrically conducting material arranged in the plurality of passages.

21. (Original) The method according to Claim 20, further comprising:

providing a space transformer connected to the electrically conducting material arranged in the plurality of passages.

22. (Original) The method according to Claim 14, wherein the external electrical path is provided between pairs of external connections on the semiconductor devices.

23. (Original) The method according to Claim 14, wherein the external electrical path is provided between a plurality of external connections on the semiconductor devices.

24. (Withdrawn) The method according to Claim 14, wherein the external electrical path is provided between non-adjacent external connections on the semiconductor devices.

25. (Withdrawn) The method for forming a structure for testing external connections to semiconductor devices, the method comprising:

providing a thin film of electrically insulating material;

providing a plurality of passages through the thin film of electrically insulating material, wherein the passages are arranged in a pattern corresponding to a pattern of external connections on the semiconductor device;

providing electrically conducting material in the plurality of passages; and

providing electrical connections between the electrically conducting material in selected passages.

26. (Withdrawn) The method according to Claim 25, wherein providing the electrical connections between the electrically conducting material in the selected passages comprises

providing electrically conducting material on the thin film of electrically insulating material between the selected passages.

27. (Withdrawn) The method according to Claim 25, wherein the selected passages are adjacent pairs.

28. (Withdrawn) The method according to Claim 25, wherein the electrical connections are provided between a plurality of passages.

29. (Withdrawn) The method according to Claim 25, wherein the electrical connections are provided between non-adjacent passages.